Reprogrammable Acquisition Architecture for Dedicated Positron Emission Tomography

Giancarlo Sportelli, *Member, IEEE*, Nicola Belcari, Pedro Guerra, *Member, IEEE*, Franco Spinella, Giovanni Franchi, Francesca Attanasi, Sascha Moehrs, Valeria Rosso, Andrés Santos, *Senior Member, IEEE*, and Alberto Del Guerra, *Senior Member, IEEE*

***Abstract*—We have developed a flexible, cost-efficient PET architecture adaptable to different applications and system geometries, such as positron emission mammography (PEM) and in-beam PET for dose delivery monitoring (ibPET). The acquisition system has been used to implement modularized dual planar detectors with very low front-end dead time, as required in PEM or in ibPET. The flexibility is obtained thanks to the FPGA-based, reprogrammable, TDC-less coincidence processor. The final goal is to propose an effective acquisition methodology and the construction of a compact, low-cost instrument able to provide early diagnosis and to improve the effectiveness of follow-up studies for smaller tumours with respect to those studied with present clinical equipment (e.g., whole-body PET, SPECT, or scintigraphy).**

***Index Terms*—Coincidence detection, data acquisition architecture, dead time, fully programmable gate array (FPGA), in-beam monitoring, latency, positron emission mammography (PEM), Stratix III.**

I. Introduction

IT IS TODAY a widely adopted practice the use of specifically tailored system geometries for small-scoped clinical imaging applications, in order to overcome the well-known fundamental limitations of whole-body positron emission tomography (PET) [1]. Most remarkable examples are brain [2], mammography [3], and, more recently, in-beam PET imaging for the monitoring of the delivered dose during hadron therapy [4] and PET probes for guided surgery [5].

Dual planar geometry has shown to be particularly convenient for both positron emission mammography (PEM) [6], [7] and ibPET [8]–[10]. Its interest is mostly due to the good results in terms of spatial resolution and sensitivity, the relatively simple detector setup and the practical advantage given by the lateral aperture which allows for CT integration, image-guided biopsy or hadron beam passage, depending on the specific application [11], [12].

Novel multianode, flat-panel, position-sensitive photomultiplier tubes (PSPMT, such as Hamamatsu H8500) allowed a general trend in increasing detector size, with consequent additional benefits in terms of spatial resolution and sensitivity, thus arising again the question on the convenience of PET over other modalities in controversial fields such as clinical primary screening or cancer staging and follow up [13], [14]. In fact, apart from the higher geometrical efficiency, large detector panels are essential in order to compensate the relatively poor resolution in the direction normal to the detector planes.

When the detection efficiency becomes high, the next important question that has to be faced is dead-time τ. In fact, the actual efficiency for a given detector material is dominated by the product of the dead time and the front surface area of the detector [15], [16]. Although it is difficult to quantify dead-time losses, state-of-the-art electronics have been demonstrated to require dead-time management in clinical imaging even for limited-angle sampling systems [7], [17]. Dead-time correction procedures have been proposed in the past [18]; they are typically based on the combination of paralyzable and nonparalyzable models, but involve a series of empirical parameters, which are affected by measurement and fitting errors. Conversely, detectors modularization has already been addressed as the most practical solution for reducing dead time [15], [16], although it requires a degree of electronics parallelization and, most notably, time to digital conversion (TDC)-based coincidence processing, that heavily weigh on overall system cost, thus hampering its applicability, specially for small dedicated PET systems.

In this paper we propose a new acquisition architecture that provides state-of-the-art performances with a low-cost approach for multichannel coincidence processing. We also present, as proof of concept implementation, a dedicated dual planar PET system, designed to accept up to nine modules per detector. The functioning concept is demonstrated with two modules per detector, and the results are extrapolated to foresee the capabilities that the full system will have once completed.

II. Detectors Geometry

A. General Description

The developed system is a dual head Positron Emission Tomograph with planar detectors. In its current version each head

Manuscript received July 23, 2010; revised December 18, 2010; accepted January 31, 2011. Date of publication March 07, 2011; date of current version June 15, 2011. This work was supported in part by the MIUR, in the framework of the PRIN2006 program, "Development of a dedicated PET tomograph for breast cancer imaging," Spain's Ministry of Science and Innovation (TEC2010-21619-C04-03 and TEC2008-06715-C02-02), Centro para el Desarrollo Tecnológico Industrial (CDTI), through the CENIT framework (AMIT project) and INNPACTO, Instituto de Salud Carlos III (PI09/91058 and PI09/91065), Comunidad de Madrid (Consejería de Educación and ARTEMIS S2009/DPI-1802), and the European Regional Development Funds (FEDER).

G. Sportelli, P. Guerra, and A. Santos are with the Biomedical Image Technologies Group, E.T.S.I.T., Universidad Politécnica de Madrid, 28040 Madrid, Spain and also with the Research Center in Bioengineering, Biomaterials and Nanomedicine (CIBER-BBN), Spain (e-mail: gsportelli@die.upm.es; andres@die.upm.es).

N. Belcari, F.Attanasi, S. Moehrs, V. Rosso, and A. Del Guerra are with the Department of Physics "E. Fermi," University of Pisa, 56127 Pisa, Italy and also with the INFN—Sezione di Pisa, 56127 Pisa, Italy (e-mail: belcari@df.unipi.it; sascha.moehrs@df.unipi.it; alberto.delguerra@df.unipi.it; francesca.attanasi@pi.infn.it; valeria.rosso@pi.infn.it; franco.spinella@pi.infn.it).

F. Spinella is with the INFN—Sezione di Pisa, 56127 Pisa, Italy (e-mail: franco.spinella@pi.infn.it).

G. Franchi is with the AGE Scientific, Capezzano Pianore, 55041 Lucca, Italy (e-mail: gfranchi@agescientific.com).

Digital Object Identifier 10.1109/TNS.2011.2113193

is composed of four modules arranged in a 2×2 matrix. Each module consists of a square 64 anodes photomultiplier tube (Hamamatsu H8500) coupled to a matrix of 23×23 LYSO scintillating crystals (1.9 mm $\times$ 1.9 mm $\times$ 16 mm pixel dimensions, with a 2.0 mm pitch). The resulting active area is 10 cm $\times$ 10 cm per head. The division of the scintillating matrix into submatrices implies a loss of active area due to the dead space between the modules. With our system the dead space between modules is about 6 mm wide. In this way we have a geometrical efficiency loss which is about 12% with respect to a solution based on a large scintillating matrix, read out by a four (2×2) tubes assembly. However, this geometrical efficiency loss is largely compensated by a gain in count rate characteristics.

In PEM and ibPET applications the distance between detectors is expected to range from 7 to 20 cm thus resulting in a solid angle of view ranging from 47% to 13% from the centre.

In order to exploit the higher efficiency of the adopted geometry, we have developed a flexible and expandable acquisition system specifically designed to work with modular detectors. The intention is to spread coincidence events and data flow among different modules, thus reducing both system dead time and the probability of electronic pile-up. Doing so, the probability for two photons to overlap remains constant even if the total detector area is increased. If the detector is subdivided into n modules of dead time t each, the resulting total dead time can be roughly estimated as $\tau_n = \tau/h_n \simeq \tau/n$, where $1/h_n$ is the fraction of the system being occupied in the acquisition of a coincidence. In fact, if we suppose that coincidences are evenly distributed among the modules, and that the dead time of the acquisition system is dominated by the contribute of modularized electronics, we can expect $h_n \simeq n$.

It is important to note that the reduction happens at single-event level, thus effectively reducing events pile-ups without any changes in the signal conditioning circuitry and for any kind of scintillating material. As a matter of fact, the scanner acquires events as if they were coming from $2n$ independent detectors, being n the number of modules per detector, while the digital controller resolves coincidences only between opposite detectors.

III. Frontend Electronics

Each detector module outputs 64 signals proportional to anode currents, used for energy and position characterization, plus a timing signal taken from the last dynode. The output signals pass through a conditioning stack made of a coding board, a pulse shape preamplifier board (PSP) and a timing board. Conditioning circuit boards have been realized with the same form factor of the scintillating crystal and the photomultiplier tube, in order to allow the whole module stack to be aligned with others to form the full detector block (Fig. 1).

The coding board consists of a Symmetric Charge Division (SCD) [19], [20] resistive network, which has been chosen for its simplicity and good performance [21]. The SCD reduces the 8×8 signals of each PMT into $8+8$ signals. The $8+8$ signals enter a passive resistive chain that further reduces the number of signals to Anger-like $2\,(x)+2\,(y)$ [21]. The last dynode signal is passed through, up to the Constant Fraction Discriminator (CFD) [22], which is the last board of the stack. The CFD generates a differential PECL trigger, after a constant delay since the crossing of a controllable fraction of each incoming pulse.

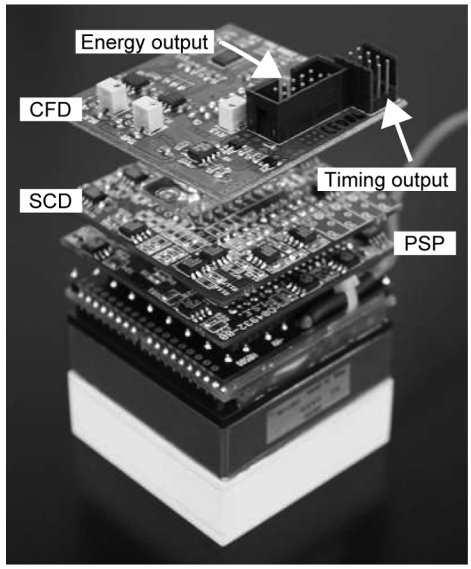


Fig. 1. Detector module. Stacked up to down are the CFD, the SCD, the PSP, the photomultiplier tube, and the LYSO crystal. The module has been implemented with a compact form factor in order to minimize detector packing dead area.

The fraction is currently set to 17% of the peak level, while the pulse discrimination threshold is kept as low as possible in order to acquire all events. The outputs of the whole module consist eventually of four analog Anger-like signals, which are sent to a Data Acquisition (DAQ) board, and a digital timing signal that goes directly to the Control FPGA for coincidence processing.

The frontend stack has already been characterized in [21].

IV. Coincidence Processing

A. Coincidence Detection

Coincidence resolution is obtained by synchronizing incoming triggers from the CFD into time bins of $1/f$, where f is the maximum available clock frequency of the target FPGA. The maximum clock speed is achieved by separating a local clock domain from the rest of the processing core inside the FPGA. Doing so the tight timing constraint of the coincidence network does not affect the more complex data processing logic. Thus a coincidence is detected whenever overlapping or contiguous bins contain one trigger each. The coincidence resolution results $3/f$, which is the maximum allowed delay for two triggers to fall into contiguous bins. Considering that FPGA available frequencies range from 300 MHz even on low-end devices to 1 GHz, this technique allows to easily resolve coincident events closer than 10 ns.

The triggering latency is composed by two main components, the synchronization latency and the processing latency. The first depends on the technological characteristics of the FPGA fabric, it is the main contribution and it is unlikely to change considerably. The second depends on the signal propagation through boards, the processing latency in terms of clock cycles and the clock period, which has been already optimized and could only slightly improve with newer FPGAs.

In our implementation, the embedded coincidence network was able to resolve coincidences with a total latency lower than 50 ns, allowing to employ peak-detector based digital

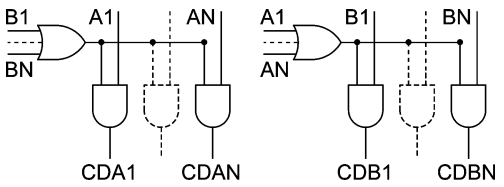


Fig. 2. Simplified schematic of the OR-AND-gating function implemented in the synchronous coincidence detection network. Ai and Bi ($i \in \{1, 2, \ldots, n\}$) are the timing inputs corresponding to the digital triggers generated by the CFDs.

conversion and process only coincident events. This reduces the amount of data to be processed by at least one order of magnitude with respect to typical TDC-based acquisition systems, in which all single events have to be acquired, characterized and eventually resolved as valid events or discarded.

As an optimal solution for the current dual geometry a symmetric synchronous gating network has been implemented, whose schematic diagram is shown in Fig. 2. An extended description of the synchronous coincidence processor can be found in [23]. Every time a trigger comes from a CFD it is shaped to a synchronous two-cycle pulse and fed to the corresponding network input Ai or Bi ($i \in \{1, 2, \ldots, n\}$). The implemented gating network has a complexity of $O(n)$, given that only one AND gate per detector module is used, plus an OR gate per detector Fig. 2. This allows to process high numbers of modules within few FPGA resources. In the more general case, where modules are not divided in two subsets and all pairs can be resolved as coincident, the gating network would have a complexity of $O(n^2)$.

It is important to note that the complexity of the gating network affects only the number of FPGA internal resources, which usually abound. In fact, the coincidence processor is synchronous, thus taking advantage of logic pipelining and generic optimization, that would be impossible with asynchronous gating. A more detailed description of the synchronous coincidence processor architecture and performances can be found in [23].

B. Random Events Estimation

Random event rates are estimated using the delayed window technique. Digital pulses from the edge detectors of one of the two sides are generated after a fixed delay, longer than the coincidence window. This allows to filter all true events thus providing a pure random trigger source. In comparison with estimating lines of response from arbitrarily randomized samples of singles, this method gives a direct quantitative estimation of the random distribution, without any *a priori* assessment of the actual coincidence window, which can be affected by systematic errors. The fixed delay is easily implemented in the FPGA by means of shift registers. The length of the window delay is an important parameter that can severely affect the coincidence resolution latency. In fact, a delayed coincidence can be resolved only after the delayed window has been received. Therefore, the analog pulses that we want to acquire, because they were resolved as valid events, have to be properly delayed with inductive delay lines in order to be converted. This is an undesirable situation: long delay lines degrade the signal-to-noise ratio and impose a tight constraint on the applicable window delay and acquisition dead time.

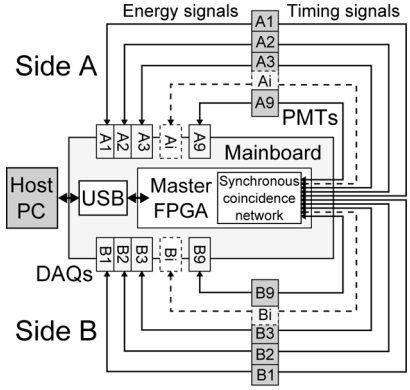


Fig. 3. Overall architecture of the acquisition system. Data connections between the DAQ boards ant the Control FPGA have been omitted for picture clarity.

In order to free the analog delay requirement, a variant of the delayed window technique has been implemented. The idea is to acquire only prompt events that are in coincidence with delayed triggers. In this way we lose events coming from the delayed side. We then implement a symmetric delayed coincidence network in which we swap delayed and prompt sides, in order to acquire prompt random events also from the other detector. This is easily achieved by replicating the network component inside the FPGA. Given that the information held by pairing prompt and delayed events is in any case random, it can be eventually reconstructed by randomly pairing events from both networks, thus achieving an equivalent number of random lines of response. Consequently, the delay constraint on energy paths described in the previous section is released, thus bringing considerable advantages to the energy resolution. The new technique has been previously proposed in [24]. In the cited work, acquisitions executed with both standard delayed window technique and its variant have been compared and have demonstrated a good distribution correlation.

V. Acquisition System

A. Overall Architecture

The acquisition system has been specifically designed for the dual modular head detectors proposed in this paper. A simplified scheme of the overall architecture is illustrated in Fig. 3. Timing signals are processed by the FPGA which keeps track of all the events and triggers the data acquisition on the DAQ boards when a valid event is detected. Event tracking is achieved by internally recording incoming events prior to their full acquisition and until they are sent to the host. This provides a robust control over pile-ups and enhances data transfer efficiency from the DAQs. DAQ boards operate independently from each other, therefore only a fraction of the system is busy during the acquisition of each coincidence. This, together with an adequate buffering on each DAQ, allows multiple simultaneous acquisitions, which is the key for dead-time reduction. The data link between DAQ boards and mainboard is obtained with two asynchronous 16-bit wide parallel buses, one each per detector side. This choice has been made in order to keep the asynchronous boundary between all involved boards, which is commonly referred to as GALS (globally asynchronous locally synchronous)

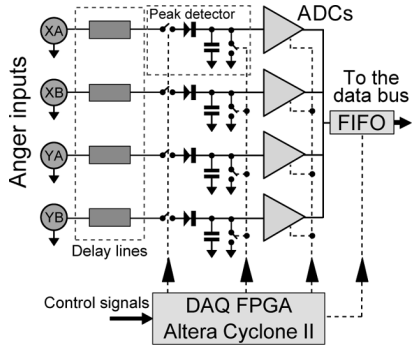


Fig. 4. Simplified schematic of the DAQ board. Its main task is to timely enable the four mounted peak detectors and register digitized peak values. Control machines and target FIFO are embedded in the Cyclone II FPGA.

system design, particularly suitable for lowering system complexity and power consumption [25]. Tests showed that proper buffering and efficient data retrieval from the DAQ boards make the bandwidth of this kind of connection well sized with respect to the rest of the system.

B. DAQ Boards

Each DAQ board mounts a Cyclone II FPGA (Altera Corp., San Jose CA), which implements buffering, bus control and triggers the four onboard peak detectors. Each peak detector, when active, follows the voltage of an incoming Anger coded signal from the PMT and holds on the highest value, which is in turn converter by a 10 MHz, 12-bit A/D converter. Peak hold and registration circuitry is enabled only after an acquisition trigger is received from the main board. In fact, the current RC peak follower could not sustain charge-discharge cycles at normal single rates. A simplified schematic of the DAQ board is shown in Fig. 4. Each DAQ board is provided with an input inductive delay pad, which is used to compensate coincidence processing latency. With the current latency of 50 ns we have observed no significant signal degradation through the delay lines. The total DAQ dead-time is composed of two main contributions: the peak waiting time and the time required by the voltage-followers capacitors to discharge. The peak waiting time is the programmable interval during which the DAQ is turned on and follows the Anger signals. This interval must be sufficiently large to assure that the energy pulses have passed through completely. Thanks to the implementation of the new delayed window technique this waiting interval can be kept as low as the length of the scintillating pulses.

C. Mainboard

The mainboard hosts a Control FPGA, it powers the whole system and provides data connection. It also provides circuitry necessary for logic translation and physical socketing for the DAQ boards (Fig. 5). The FPGA streams data to the Host PC at 480 Mb/s through an USB 2.0 controller (CY7C68013A, Cypress Semiconductor Corp., San Jose, CA), and is connected asynchronously to the coincidence and DAQ boards. The FPGA is a high-end model (Stratix III, Altera Corp., San Jose, CA) which provides high memory resources, needed for data buffering, high I/O pin count and low propagation delays, required for prompt coincidence monitoring.

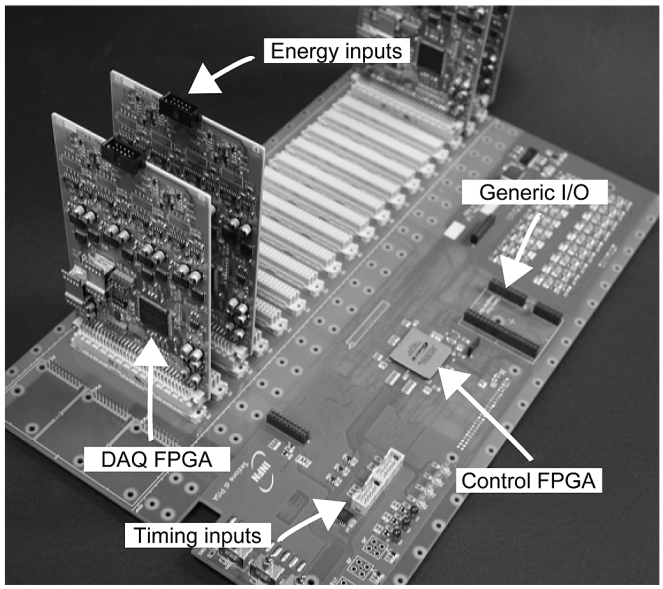


Fig. 5. Mainboard. In the picture only four DAQ boards have been connected. The current acquisition implementation is already capable of handling up to 18 boards.

TABLE I
REQUIRED I/O RESOURCES FOR THE CONTROL FPGA

Purpose	FPGA pins	Multiplier
DAQ transfer control	3	per module
DAQ trigger control	2	per module
CFD trigger	1	per module
Data bus	16	per bus
Generic interface I/O	~ 50	1

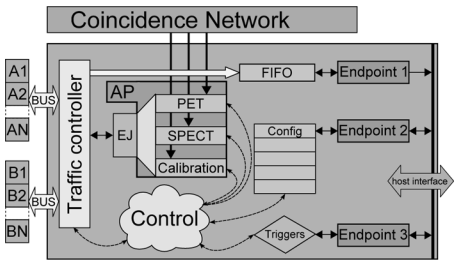


Fig. 6. Simplified scheme of the firmware architecture of the Control FPGA. The AP can work in coincidence (PET), single (SPECT), and calibration modes.

The current mainboard represents only a possible implementation of the more general acquisition architecture. The I/O requirements for the FPGA account for a total of 6 pins per module plus roughly 100 general-purpose single-ended I/O (Table I), thus allowing to manage tens of modules with a single high-end FPGA.

VI. DIGITAL CONTROL

The main processing tasks carried out by the Control FPGA, consist of data transfer management, event tracking, run-time configuration and status control. A simplified scheme of main FPGA firmware is reproduced in Fig. 6. Event processing has

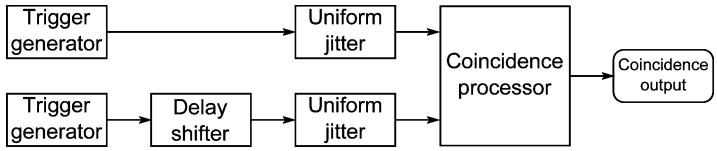


Fig. 7. Simplified diagram of the VHDL testbench used to simulate the coincidence detection efficiency of the synchronous coincidence processor.

been divided into two main stages in pipeline: the traffic controller (TC) and the acquisition processor (AP). The AP-TC pipelining maximizes the efficiency of data retrieval from the DAQ boards, and allows for more complexity in the digital processing part of the AP. The AP consists of a common container interface, in which different dedicated controllers, i.e., coincidence (PET), single (SPECT), calibration and debug acquisition controllers, can be switched in run-time. In this way the timing budget can be efficiently exploited for each acquisition modality, at the cost of major logic resources usage.

An event journal (EJ) is the only interface between the AP and the TC. The AP, according to a set of programmable rules, processes incoming triggers from the coincidence network, generates the outputs that trigger the interested DAQs, and writes event records into the EJ. Each record contains information on pile-ups, scattered and random coincidences. Events are marked as pile-ups when their correspondent triggers are sufficiently separated to be resolved by the CFD but closer than a specified timing window, that is adjusted to the length of energy pulses. The TC pops the records, downloads acquired data from DAQ buses and merges the event record information. This kind of real-time data manipulation and pipelining implies various advantages. Acquisition policies can be implemented in the firmware in a modular manner that minimizes the dead-time in terms of clock cycles per event. Moreover, new conditions and experimental behaviors can be easily merged in the current state machines. Digital processing can also be inserted, in the AP-TC path, in order to alleviate off-line processing, without affecting dead-time or data throughput.

VII. Results

A. Timing Resolution

Timing resolution has been simulated and experimentally measured for the reference clock frequency of 288 MHz. A simplified diagram of the simulated testbench is showed in Fig. 7. The *delay shifter* introduces a systematic delay between the two generated triggers in order to explore any delay possibility. For each delay shift the trigger is repeated for a high number of times with an applied uniform random jitter to prevent any kind of phase-to-clock biasing effect. The number of coincidences detected per generated triggers is counted and plotted.

Experimental measurement has been done in a very similar way with respect to the simulation. A function synthesizer has been used in order to generate a train of pulses at a specific frequency. The generated pulses were used to emulate CFD outputs and fed to the FPGA pins correspondent to the coincidence processor inputs. The detection efficiency has been then derived by relating the coincidence rate reported by the control software with the singles rate and the imposed pulse frequency.

Measurements results are showed in Fig. 8. The FWHM for the simulated case is 10.4 ns, which is exactly $3\tau = 3/f$, where

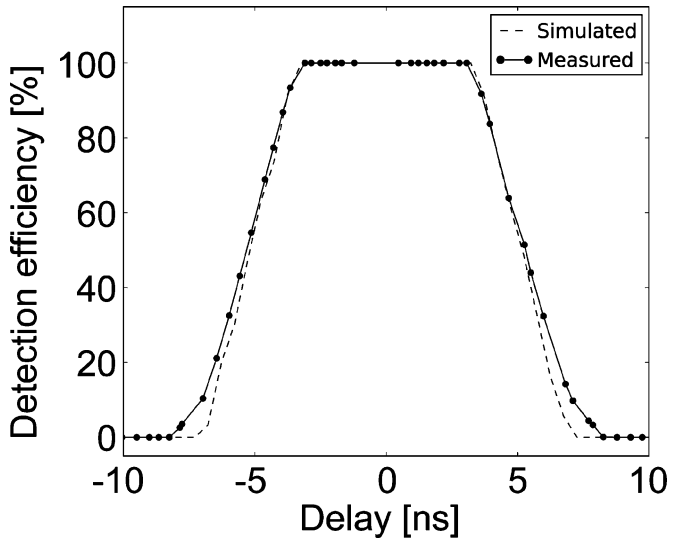


Fig. 8. Simulated and experimental detection efficiency of the synchronous coincidence processor.

$f = 288$ MHz is the applied clock frequency. Experimental measurements show a delay offset of about 1.2 ns between the two opposing sides and an efficiency FWHM of 9.1 ns. The small offset can be easily corrected by adjusting the length of trigger cables or employing the embedded delay taps available at the input buffers of the FPGA.

B. Pixel Identification and Energy Resolution

Acquisitions of a planar FDG source have been conducted to measure pixel identification capabilities. The obtained flood image on one of the detector modules, is reported in Fig. 9. The image has been obtained by irradiating the detectors with roughly 40 million events per module. All the modules show similar maps. In the image, pixels are well separated and can be clearly resolved, with some exceptions at the borders. The energy histogram of all coincidences in one module is shown in Fig. 10. The histogram has been obtained by separately correcting each pixel for its own conversion efficiency. The achieved energy resolution is 20% FWHM, with a minimum energy resolution per single pixel of 15% FWHM, both values comparable with the same obtained in similar PET systems [26], [27]. A long tail can be appreciated in the obtained histogram, that we ascribe as an effect of the optical absorption characteristic of the scintillating crystals used in our tests. This effect has been previously studied and simulated for the used detector modules [28].

C. Dead-Time Measurements

We calculated the dead time τ of constant fraction discriminators with the method of the two sources [29] using one and two

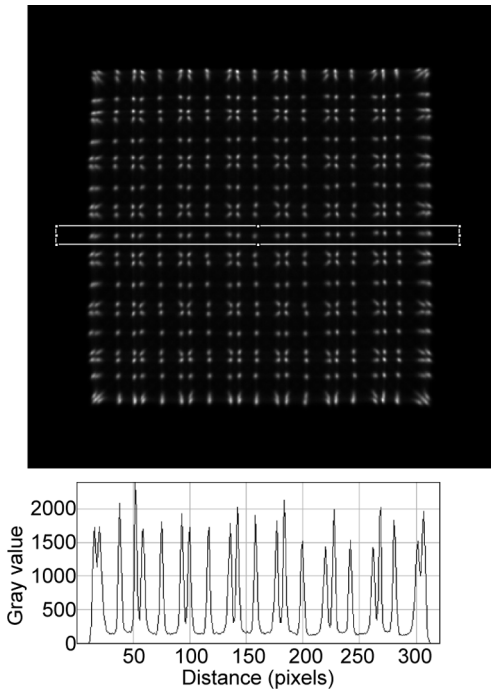


Fig. 9. Flood image of one of the detector modules (top) and plot of the horizontal section of a pixel row (bottom). Flood images on all modules appear similar. The map has been obtained binning roughly 40 million events in a 400×400 pixels image, acquired from a FDG-filled planar source during 40 min.

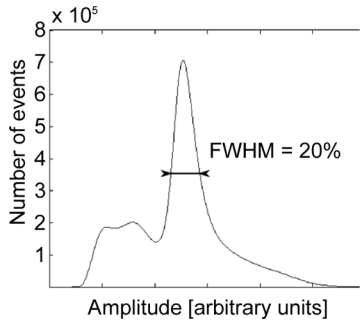


Fig. 10. Global energy histogram calculated on all acquired coincidences. The histogram has been obtained by summing separately corrected energy histograms on each pixel. The long tail is an effect of the optical attenuation characteristic of the scintillating crystals used in our tests. It represents a fraction of the 511 keV photons that were less attenuated in their path inside the crystal pixel toward the PMT.

modules per detector. In our experiment we used two small capsules filled with equal amounts of FDG, centred in the FOV of the 1 versus 1 and 2 versus 2 assemblies. This method allows to make an approximate estimation of the dead time of a counting system by comparing counting rates of two sources when examined separately and together. For paralyzable counting systems, the estimation formula is

$$\tau = \left[\frac{2R_{AB}}{(R_A + R_B)^2}\right] \ln\left[\frac{(R_A + R_B)}{R_{AB}}\right] \tag{1}$$

where R_A, R_B, and R_{AB} are the count rates of the two sources separately and together, respectively. The experiment was carried out with detectors facing 8 cm apart and two identical small capsules of FDG. It is important to note that with this experiment

TABLE II
TWO SOURCES EXPERIMENT RESULTS FOR THE ESTIMATION OF CFD DEAD TIME WITH 1 AND 2 MODULES PER DETECTOR

Modules	R_A	R_{AB}	R_B	τ
1 vs 1	235 kHz	438 kHz	231 kHz	246 ns
2 vs 2	420 kHz	790 kHz	419 kHz	138 ns

TABLE III
EXPERIMENT RESULTS FOR THE ESTIMATION OF ACQUISITION SYSTEM DEAD TIME WITH 1 AND 2 MODULES PER DETECTOR

Modules	R_I	R_O	T
1 vs 1	57 kHz	55 kHz	564 ns
2 vs 2	127 kHz	122 kHz	364 ns

we did not want to characterize the single front-end module, which is still susceptible for improvements, but rather the relationship between the detectors as a whole, when composed of only one or two modules. The obtained results are summarized in Table II, the obtained dead-time reduction factor for front-end electronics is $h_{\mathrm{CFD},2} = 1.78$.

With the same setup we calculated the dead time T of the acquisition system by comparing the number of input coincidences R_I with the number of coincidences actually recorded R_O. The values of R_I and R_O are counted inside the control FPGA and provide an exact estimation of input and output rates. The calculation is performed using the nonparalyzable model, given that coincidence triggers that can not be attended are simply ignored. The used formula is as follows:

$$T = \frac{(R_I - R_O)}{(R_O R_I)}. \tag{2}$$

The obtained results are summarized in Table III. It results that acquisition dead time is reduced by a factor $h_{\mathrm{ACQ},2} = 1.55$.

D. Estimation of the Combined Transfer Function

In order to obtain a preliminary validation of the modular approach, we derived a transfer function model, that we use as a qualitative assessment of system counting capabilities. In our model, the transfer function of the system as a whole is determined by

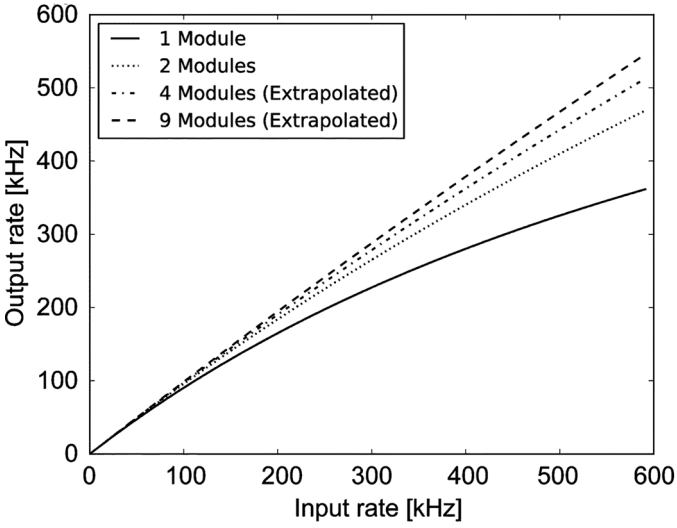
- front-end dead time τ, paralyzable;
- cCoincidence network dead time, negligible;
- acquisition system dead time T, nonparalyzable;
- loss factor F, due to the CFD discrimination efficiency.

A system of this type has been modelled in [30]. The used model is as follows:

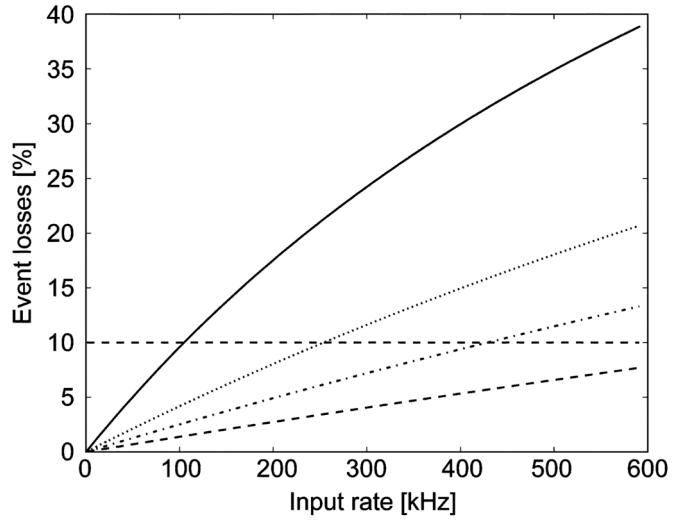
$$R \approx \frac{FNe^{-N\tau}}{1 + FNe^{-N\tau}(T - \tau)}. \tag{3}$$

The acquisition dead time is composed by the coincidence processing dead time, the event A/D conversion, and the time spent to stream data to the host computer. However, the acquisition pipeline allows to limit the total dead time to the slowest of these processes, i.e., the A/D conversion.

The value of the F factor depends on the pulse discriminating technique and its value will be assessed in further studies, for the scope of this paper it can be approximated to 1. In the transfer



(a)



(b)

Fig. 11. Comparison between the acquisition efficiency of the system between the configurations with 1, 2, 4, and 9 modules per detectors. Data about the 4 and 9 modules configurations has been extrapolated from the comparison between the 1 and 2 modules versions. (a) Total transfer function. (b) Event losses.

model, we have neglected losses due to the data throughput between the mainboard and the host computer, because the USB channel showed to be able to transfer at event rates up to 1 MHz with a dead time that could be completely compensated with available buffers and multithreading disk storage. In Fig. 11(a) plots of transfer functions for the system in the 1 versus 1 and 2 versus 2 configurations have been reported, and the expected behavior for the 4 versus 4 and 9 versus 9 implementations have been extrapolated.

The extrapolation has been done by repeatedly applying the dead-time reduction observed comparing the 1 versus 1 and the 2 versus 2 assemblies. In this way we derived the formula $h_n \simeq h_2^{log_2 n}$ with which we estimated the expected reduction for the next versions 4 versus 4 and 9 versus 9.

VIII. Conclusion

We have built a flexible and expandable data acquisition system for a dual head planar PET system, capable of detecting gamma rays from two multiple-PSPMT plates. The system is capable of managing up to 18 modules, thus allowing implementations with up to 3×3 modules per detector. At the current state it has been equipped with two detectors of 2×2 modules each, for a total area of 10 cm $\times$ 10 cm per detector. An early characterization has been carried out, by enabling only two of the four available modules per detector, and comparing the results with those obtained with a 1 versus 1 assembly. Event acquisition performances have been then predicted for the case of four and nine modules per detector. The scanner presents optimized counting characteristics, which are expected to improve overall image signal-to-noise properties. Dead-time reduction is a direct consequence of the possibility of handling parallel independent tiles per each detector, although the acquisition processors are also capable of detecting pile-ups on a single module in certain conditions. We observed a reduction in pulse discrimination dead time of 1.78, and a reduction in acquisition dead time of 1.55 for the 2 versus 2 detector assembly, with respect to the single module assembly. We then expect similar reduction factors for the bigger assemblies we are realizing. The novelty introduced is a cost-efficient in-depth modularity, obtained by parallelizing the frontend electronics and integrating the coincidence processor inside a single FPGA. Special effort has been made in order to relieve the cost dependence on the number of detectors. Conversely, data processing has been centralized in order to eliminate the need of distributed clock networks or expensive data links, without having to compromise the performance. The system requires no distributed clocks, a high-end FPGA for acquisition control and a series of off-the-shelf components for DAQ boards and front-end electronics. Although tests of the system are still at an early stage, extrapolated data show how the final system could maintain event losses below 10% for activity rates up to 500 kHz, while the streaming bandwidth allows a maximum acquisition rate of 1 MHz. As a result the system shows to be capable of state-of-the-art performance with a very low cost and low power consumption. Because of its modularity, by changing the combinatorial network logic, the system can be used for PET systems with different geometries such as ring scanners, too.

Acknowledgment

The authors would like to thank Altera Corp. for providing the Stratix III devices used for the first prototypes.

References

[1] W. Moses and J. Qi, "Fundamental limits of positron emission mammography," *Nucl. Instrum. Meth. A*, vol. 497, no. 1, pp. 82–89, 2003.
[2] F. van Velden *et al.*, "HRRT versus HR+ human brain pet studies: An interscanner test-retest study," *J. Nucl. Med.*, vol. 50, no. 5, pp. 693–693, 2009.
[3] C. J. Thompson, "Instrumentation for positron emission mammography," *PET Clinics*, vol. 1, no. 1, pp. 33–38, 2006.
[4] T. Nishio *et al.*, "Dose-volume delivery guided proton therapy using beam on-line pet system," *Med. Phys.*, vol. 33, no. 11, pp. 4190–4197, 2006.
[5] A. Studen *et al.*, "Timing performance of the silicon PET insert probe," *Radiat. Prot. Dosim.*, vol. 139, no. 1–3, pp. 199–203, 2010.
[6] C. J. Thompson *et al.*, "Feasibility study for positron emission mammography," *Med. Phys.*, vol. 21, pp. 529–529, 1994.
[7] R. R. Raylman *et al.*, "The positron emission mammography/tomography breast imaging and biopsy system (PEM/PET)," *Phys. Med. Biol.*, vol. 53, no. 3, pp. 637–653, 2008.

[8] W. Enghardt *et al.*, "Charged hadron tumour therapy monitoring by means of PET," *Nucl. Instrum. Meth. A*, vol. 525, no. 1–2, pp. 284–288, 2004.
[9] F. Attanasi *et al.*, "Experimental validation of the filtering approach for dose monitoring in proton therapy at low energy," *Phys. Medica*, vol. 24, no. 2, pp. 102–106, 2008.
[10] S. Vecchio *et al.*, "A pet prototype for in-beam monitoring of proton therapy," *IEEE Trans. Nucl. Sci.*, vol. 56, no. 1, pp. 51–56, 2009.
[11] I. Weinberg *et al.*, "Applications of a PET device with 1.5 mm FWHM intrinsic spatial resolution to breast cancer imaging," in *Proc. IEEE ISBI 2004 Conf.*, pp. 1396–1399.
[12] W. A. Berg *et al.*, "High-resolution fluorodeoxyglucose positron emission tomography with compression is highly accurate in depicting primary breast cancer," *Breast J.*, vol. 12, no. 4, pp. 309–323, 2006.
[13] H. Zaidi and C. Thompson, "Evolution and developments in instrumentation for positron emission mammography," *PET Clinics*, vol. 4, no. 4, pp. 317–327, 2009.
[14] W. Berg *et al.*, "High-resolution fluorodeoxyglucose positron emission tomography with compression is highly accurate in depicting primary breast cancer," *Breast J.*, vol. 12, no. 4, pp. 309–323, 2006.
[15] W. Moses *et al.*, "PET detector modules based on novel detector technologies," *Nucl. Instrum. Meth. A*, vol. 353, no. 1–3, pp. 189–194, 1994.
[16] R. Raylman *et al.*, "Quantification of radiotracer uptake with a dedicated breast PET imaging system," *Med. Phys.*, vol. 35, no. 11, pp. 4989–4989, 2008.
[17] L. MacDonald *et al.*, "Clinical imaging characteristics of the positron emission mammography camera: PEM flex solo II," *J. Nucl. Med.*, vol. 50, no. 10, pp. 1666–1666, 2009.
[18] M. Daube-Witherspoon and R. Carson, "Unified deadtime correction model for PET," *IEEE Trans. Med. Imag.*, vol. 10, no. 3, pp. 267–275, 1991.
[19] P. Olcott *et al.*, "Compact readout electronics for position sensitive photomultiplier tubes," *IEEE Trans. Nucl. Sci.*, vol. 52, no. 1, pp. 21–27, 2005.
[20] V. Popov *et al.*, "Analog readout system with charge division type output," in *Proc. IEEE NSS/MIC 2001 Conf.* , vol. 4, pp. 1937–1940.
[21] N. Belcari *et al.*, "Performance of a four-output front-end electronics for multi-anode PMTS readout of scintillator arrays," *Nucl. Instrum. Meth. A*, vol. 572, pp. 335–337, 2007.
[22] V. T. Jordanov and G. F. Knoll, "Digital synthesis of pulse shapes in real time for high resolution radiation spectroscopy," *Nucl. Instrum. Meth. A*, vol. 345, no. 2, pp. 337–345, 1994.
[23] G. Sportelli *et al.*, "Low-resource synchronous coincidence processor for positron emission tomography," *Nucl. Instrum. Meth. A*, 2010, accepted for publication.
[24] N. Belcari *et al.*, "A novel random counts estimation method for pet using a symmetrical delayed window technique and random single event acquisition," in *Proc. IEEE NSS/MIC Conf.*, Nov. 2009, pp. 3611–3614.
[25] A. Hemani *et al.*, "Lowering power consumption in clock by using globally asynchronous locally synchronous design style," in *Proc. ACM/IEEE Design Automation Conf.*, 1999, pp. 873–878.
[26] R. R. Raylman *et al.*, "Development of a dedicated positron emission tomography system for the detection and biopsy of breast cancer," *Nucl. Instrum. Meth. A*, vol. 569, no. 2, pp. 291–295, 2006.
[27] Y. Zhang *et al.*, "The system design, engineering architecture, and preliminary results of a lower-cost high-sensitivity high-resolution positron emission mammography camera," *IEEE Trans. Nucl. Sci.*, vol. 57, no. 1, pp. 104–110, 2010.
[28] D. Bonifacio *et al.*, "A time efficient optical model for GATE simulation of a LYSO scintillation matrix used in PET applications," *IEEE Trans. Nucl. Sci.*, vol. 57, no. 5, pp. 2483–2489, 2010.
[29] S. R. Cherry *et al., Physics in Nuclear Medicine*. Philadelphia, PA: Saunders, 2003, pp. 181–182.
[30] R. Wicks and M. Blau, "The effect of window fraction on the deadtime of anger cameras: Concise communication," *J. Nucl. Med.*, vol. 18, no. 7, pp. 732–732, 1977.