

A flexible acquisition system for modular dual head Positron Emission Mammography

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Abstract— We have developed a dedicated scanner for Positron Emission Mammography, equipped with a new detection architecture that enhances its flexibility and reduces dead time. The scanner is going to use Luthetium based scintillators, which offer good detection efficiency, and a novel modular acquisition system, capable of sustaining the high scintillation rate and being less sensitive to background radiation. The final goal is the construction of an instrument able to provide an early diagnosis and to improve the effectiveness of follow-up studies for smaller tumours with respect to those studied with present clinical equipment (e.g. PET, SPECT or scintigraphy) so as to be able to visualize and characterize breast lesions with diameters < 5 mm.

I. INTRODUCTION

AFTER 15 years since the introduction of Positron Emission Mammography (PEM) by Thompson *et al* [1], the interest on the application of the PET technique for breast cancer imaging is still high. A PEM system is usually made of a pair of planar detectors that can compress the breast. A number of PEM prototypes has been proposed with this geometry. A system utilizing two sets of scanning planar detectors has also been developed [2]. The advent of multi anode flat panel photomultiplier tubes (such as Hamamatsu H8500) has helped the development of large area planar detectors. Breast tomography is also possible with detectors that are large enough (e.g. $15\text{ cm} \times 15\text{ cm}$) [3,4].

With this geometry the system has strong count rate requirements. With the dual head planar geometry each detector head subtends a large solid angle for detecting annihilation γ -rays. Hence it is exposed to a large γ -ray flux both coming from the breast fraction within the FOV and from

regions outside the FOV. In particular a strong background is expected to come from the tracer uptake in the thorax region, for instance in the heart myocardium. In this way a high single count rate can be expected in each detector. For this reason the electronic pile-up could be a strong limitation if the detector head is read out as a single detector. In addition, the minimization of the electronic dead time is critical for the maximization of the actual system efficiency.

II. SCANNER CONCEPT

The developed system is a dual head Positron Emission Mammograph with planar detectors, whose active area in the current version is about $10\text{ cm} \times 10\text{ cm}$.

Each head is made up of a matrix with 2×2 independent detector modules. The modules are comprised of a square 64 anodes photomultiplier tube (Hamamatsu H8500) coupled to a matrix of 23×23 LYSO scintillating crystals ($1.9\text{ mm} \times 1.9\text{ mm} \times 16\text{ mm}$ pixel dimensions, with a 2.0 mm pitch).

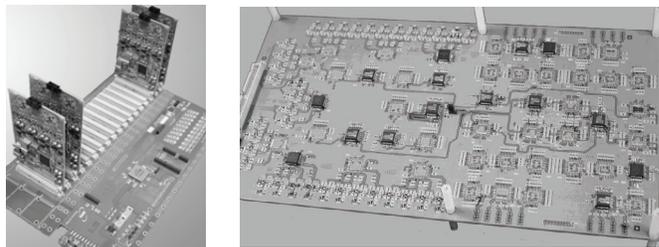


Figure 1. The PEM motherboard with four plugged DAQs (left) and the coincidence board (right).

The division of the scintillating matrix into submatrices implies a loss of active area due to the dead space between the modules. With our system the dead space is about 6 mm. In this way we have a geometrical efficiency loss which is about 12% with respect to a solution based on a large scintillating matrix, read out by a four (2×2) tubes assembly.

However, this geometrical efficiency loss can be largely compensated by a gain in count rate characteristics. For this reason we have developed a flexible and expandable acquisition system specifically designed to work with modular detectors. A first advantage of this modular approach consists in the spreading of the coincidence events, and then the data flow, among the modules, thus reducing both system dead time and the probability of electronic pile-up. In fact, if the

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head is subdivided into n modules the gain in dead time reduction can be estimated as a factor

$$f_{dead} = \frac{n^2}{n^2 - (n-1)^2}$$

i.e. the inverse of the fraction of the system being occupied in the acquisition of a coincidence event (this is strictly true for a uniform distribution of the coincidence count rate on the detector head).

With our present system with 4 + 4 modules we can achieve a reduction of the dead time by a factor $f_{dead} = 2.3$ (calculated as $f_{dead} = 4^2 / (4^2 - 3^2)$). By enlarging the system up to 9 + 9 modules the actual gain in system dead time will be of about 4.8 ($f_{dead} = 9^2 / (9^2 - 8^2)$). In addition, the division of the head into n modules helps in the reduction of the electronic pile-up by reducing the singles count rate by an equal factor n .

For this reason for each module an independent data acquisition (DAQ) board is used (Figure 1).

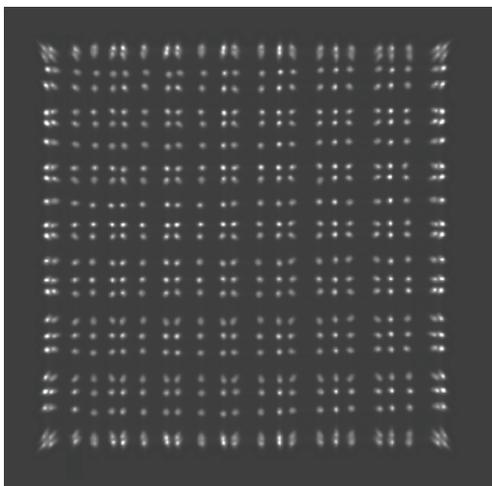


Figure 2. Flood field image of a single module irradiated with 511 keV gamma rays. All of the 23 × 23 pixels are well separated.

III. FRONTEND

A multiplexed setup based on Symmetric Charge Division (SCD) [5] resistive networks has been chosen for the readout of each individual PMT [6] as the best compromise between performances and simplicity. The SCD resistive network reduces the 8 × 8 signals of each PMT to 8 + 8 signals. The 8 + 8 signals enter a passive resistive chain that further reduces the number of signals to Anger-like 2 (x) + 2 (y) signals. The signals are then pre-amplified and sent to a DAQ board with four analogue inputs. Figure 2 shows the pixel map obtained decoding the acquires signals. The timing signal for the coincidence is generated with a constant fraction discriminator mounted on each module [7].

IV. COMBINATORIAL NETWORK

The key part of the acquisition is the combinatorial network designed to detect the time coincidence and trigger the acquisition system. In our system each module is put in time

coincidence with every module of the opposing head. Coincidences are detected by means of fast PECL AND gates connected to any allowed pair of modules (n^2). The outputs generated are a set of coincidence flags that are sent to the main FPGA. According to flags combinations and sequences, acquisition triggers are generated for the interested DAQ boards. Thanks to the wired-OR capability of the emitter-coupled logic, the logic cost has been reduced from $O(n^2)$ to $O(n)$, thus allowing to implement up to 9 modules per head, with a power consumption below 130 W.

The network is also designed for random event estimation using one of two different delayed window techniques. The first technique, which we call *conservative*, is to estimate random counts by delaying incoming triggers from one detector plate. In this way, energy pulses associated with the delayed triggers must also be delayed, by means of inductive delay lines, in order to be sampled. With the other technique, which we call *innovative*, incoming triggers are branched and delayed on both sides, thus allowing to acquire prompt energy pulses from both plates. The innovative delayed technique is explained in detail and discussed in [8].

V. ACQUISITION ARCHITECTURE

A simplified scheme of the overall architecture is illustrated in Figure 3. Each detector has a timing and an energy output. The timing output is decoded into the coincidence network, which resolves both prompt and delayed coincidences. The energy output goes directly to the corresponding DAQ boards.

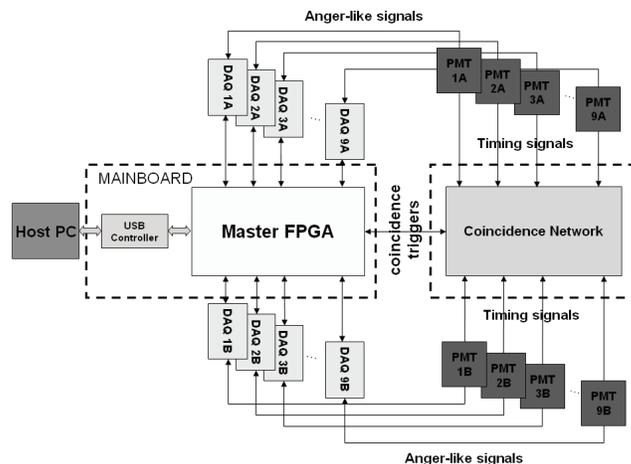


Figure 3. Simplified scheme of the acquisition architecture.

Coincidence triggers generated from the fast-AND network are processed by the FPGA which keeps track of past events and triggers the interested DAQ for energy acquisition. Event tracking provides a robust control over pile-ups and enhances data transfer efficiency from the DAQs.

The DAQ boards operate independently from each other, therefore only a fraction of the system is busy during the acquisition of each coincidence, thus allowing multiple simultaneous acquisitions.

Fetches data is then buffered and streamed to the Host PC through the USB controller. A dedicated software has been developed for data storage, real time system monitoring and configuration.

VI. MATERIALS AND METHODS

Each DAQ board is controlled by a Cyclone II FPGA (Altera Corp., San Jose CA), and implements four peak detectors. The DAQ boards convert signals from the PMT's with four 12 bit ADCs. The results of the conversion are stored in an interfacing FIFO accessible by the mainboard (Figure 4).

The mainboard is equipped with a more powerful FPGA (Stratix III, Altera Corp.) which manages data transfers, event tracking, configuration and status control. This FPGA is also connected to the USB 2.0 chip (CY68013A FX2LP, Cypress Semiconductor), and acts as a gateway between the Host PC and the acquisition system.

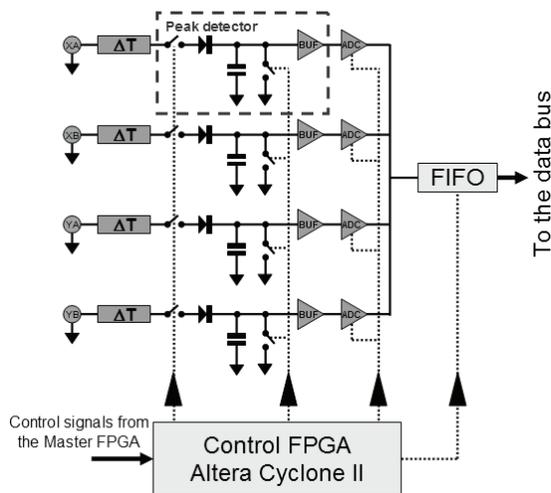


Figure 4. Scheme of the DAQ board.

The main FPGA must have enough internal memory to buffer incoming data from the coincidence network and all the DAQs, and must be fast enough to send acquisition triggers in time to fetch energy peaks. A simplified scheme of main FPGA firmware is reproduced in Figure 5.

The host configures firmware components through the control interface and a set of registers. It then triggers the acquisition and polls the FIFO for incoming data.

The events processing has been divided into two main domains: the traffic controller (TC) and the acquisition processor (AP). The AP can be switched between coincidence (PET), single (SPECT) and calibration (i.e. pedestal) modes. An *event journal* (EJ, not in the picture) is the only interface between both domains.

The AP, according to a set of programmable rules, processes incoming triggers from the coincidence network, generates the outputs that trigger interested DAQs, and writes event records into the EJ. Each record contains information on pile-ups, scattered and random coincidences. The TC pops the

records, fetches and merges data from the two DAQ buses with the event record information.

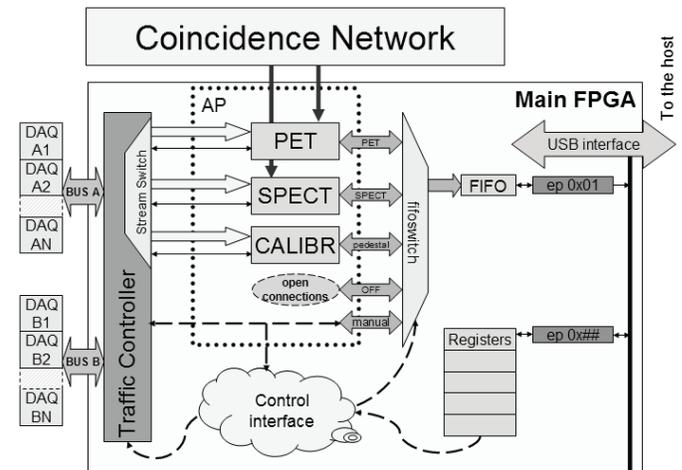


Figure 5. Simplified scheme of main FPGA firmware.

This kind of process pipelining allows to implement different specialized acquisition policies in a modular manner into the AP. New conditions and different behaviors can be then easily “plugged” and experimented. Moreover, the dead-time in terms of clock cycles per event is minimized. Finally, digital filters can also be inserted, in the TC-AP path, in order to alleviate off-line processing, without affecting dead-time or data throughput.

Acquisition tests showed that each DAQ board can produce event packets at 1 MHz, which means that coincidences could be acquired at a rate up to 9 MHz in ideal conditions (i.e. if 9 coincident pairs hit all the 18 modules at the same time). However, currently the Host-USB subsystem can sustain data throughputs up to 20 MB/s, which corresponds to a maximum coincidence acquisition rate of 1 MHz, given that the coincidence data packet size is 20 bytes.

Fine-tuning at the Host side is expected to markedly improve the current acquisition rate, which is already at the condition of state of the art [9].

VII. CONCLUSIONS

We have built a flexible and expandable data acquisition system for a dual head planar PEM system. The system has been constructed with 2×2 plates, but it is suitable for an expansion to 3×3 plates. The novelty introduced is an in-deep modularity within a planar detector geometry. This introduces the advantages of lower dead-time, less pile-ups and great digital processing capabilities, which are expected to improve overall NEC properties. Although thorough tests of the system as a whole are still in an early stage, measurements on sub-parts demonstrated that it is capable of a maximum count rate of about 1 MHz, well above the count rate requirements for PEM. Because of its modularity, an appropriate change of the combinatorial network logic could allow the acquisition to be used for PET systems with different geometries such as ring

scanners, too. Finally, the acquisition system can also work in SPECT modality with no hardware changes.

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